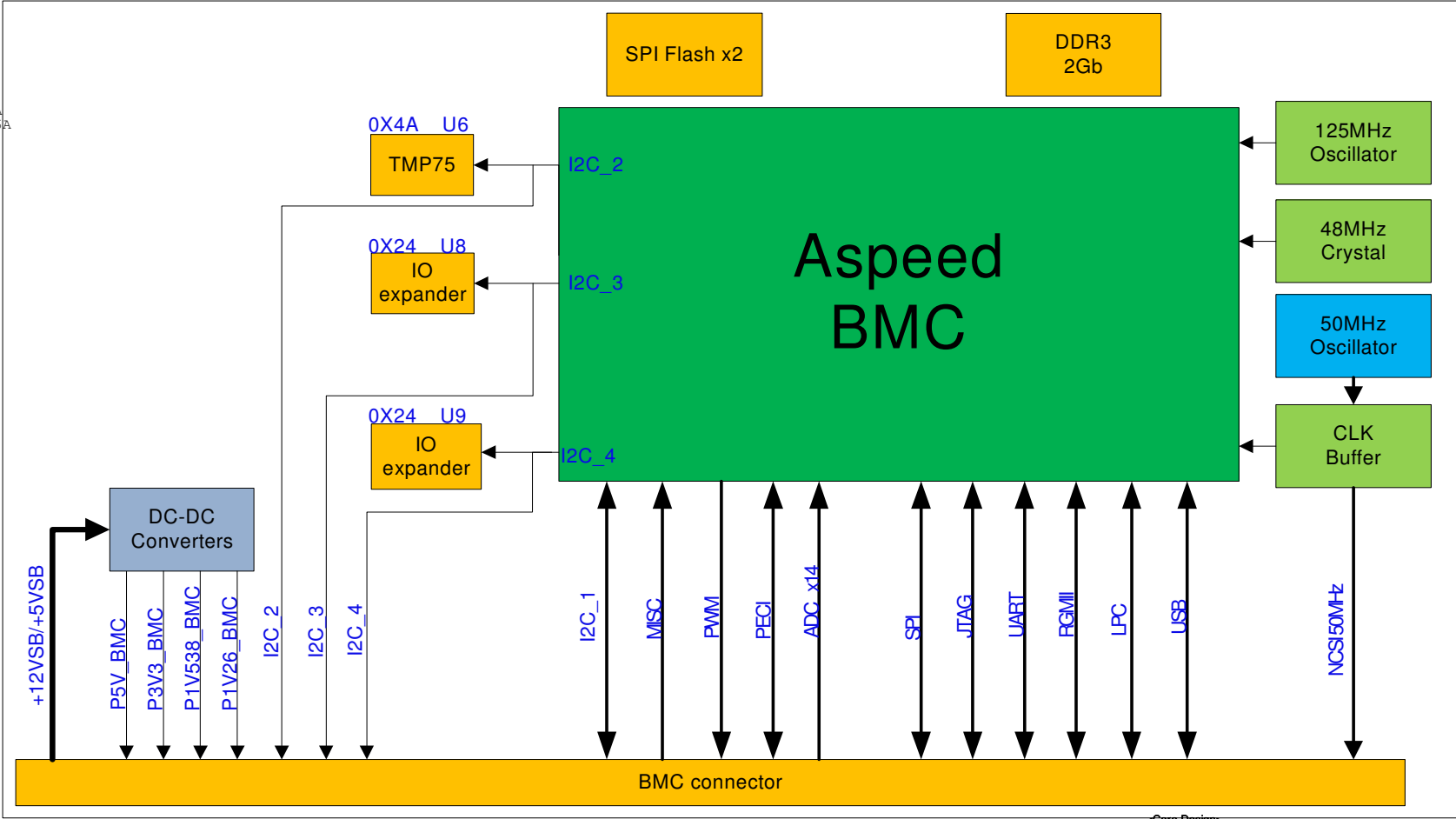


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<Core Design>



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Title

1.Block Diagram

Document Number:
PCB P/N:

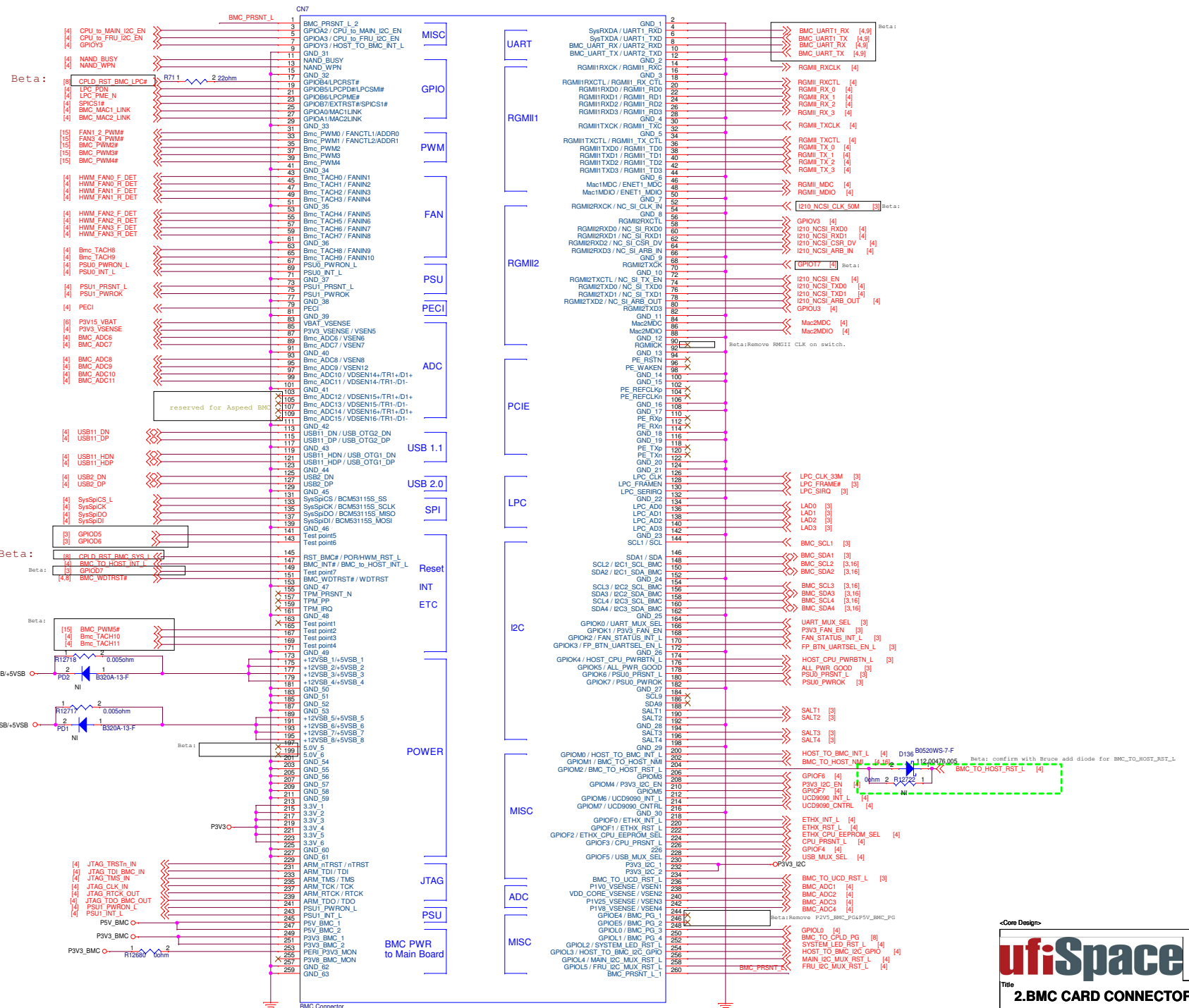
T77O925T17

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Rev

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Title

2.BMC CARD CONNECTOR

Document Number:

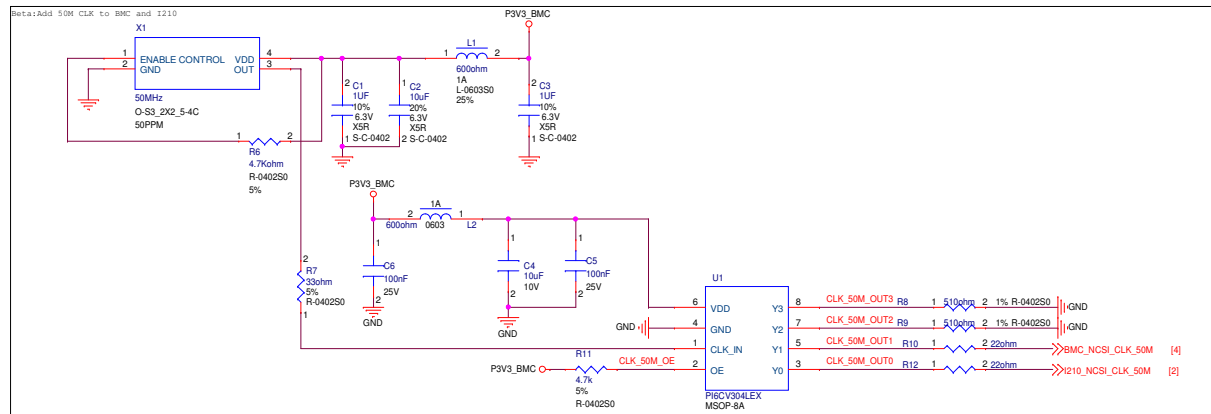
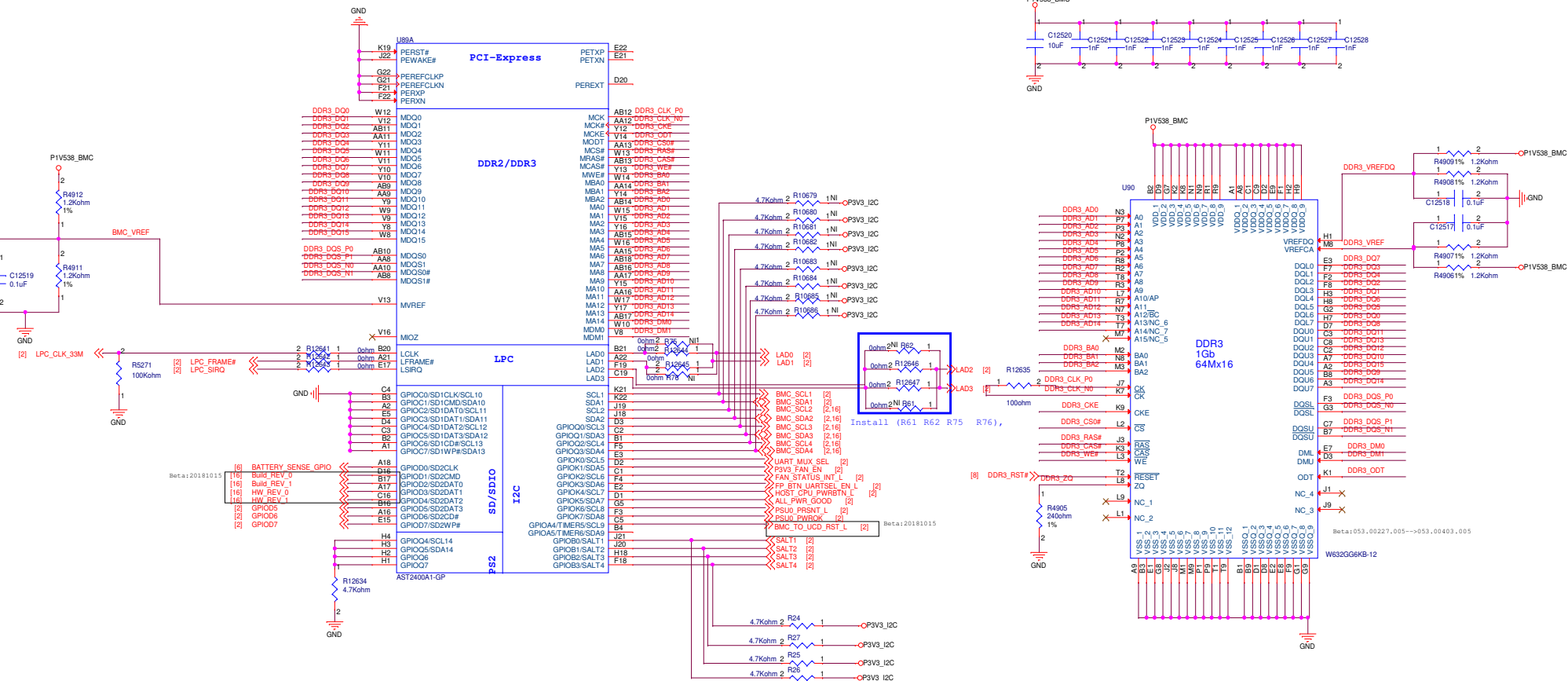
T770825117

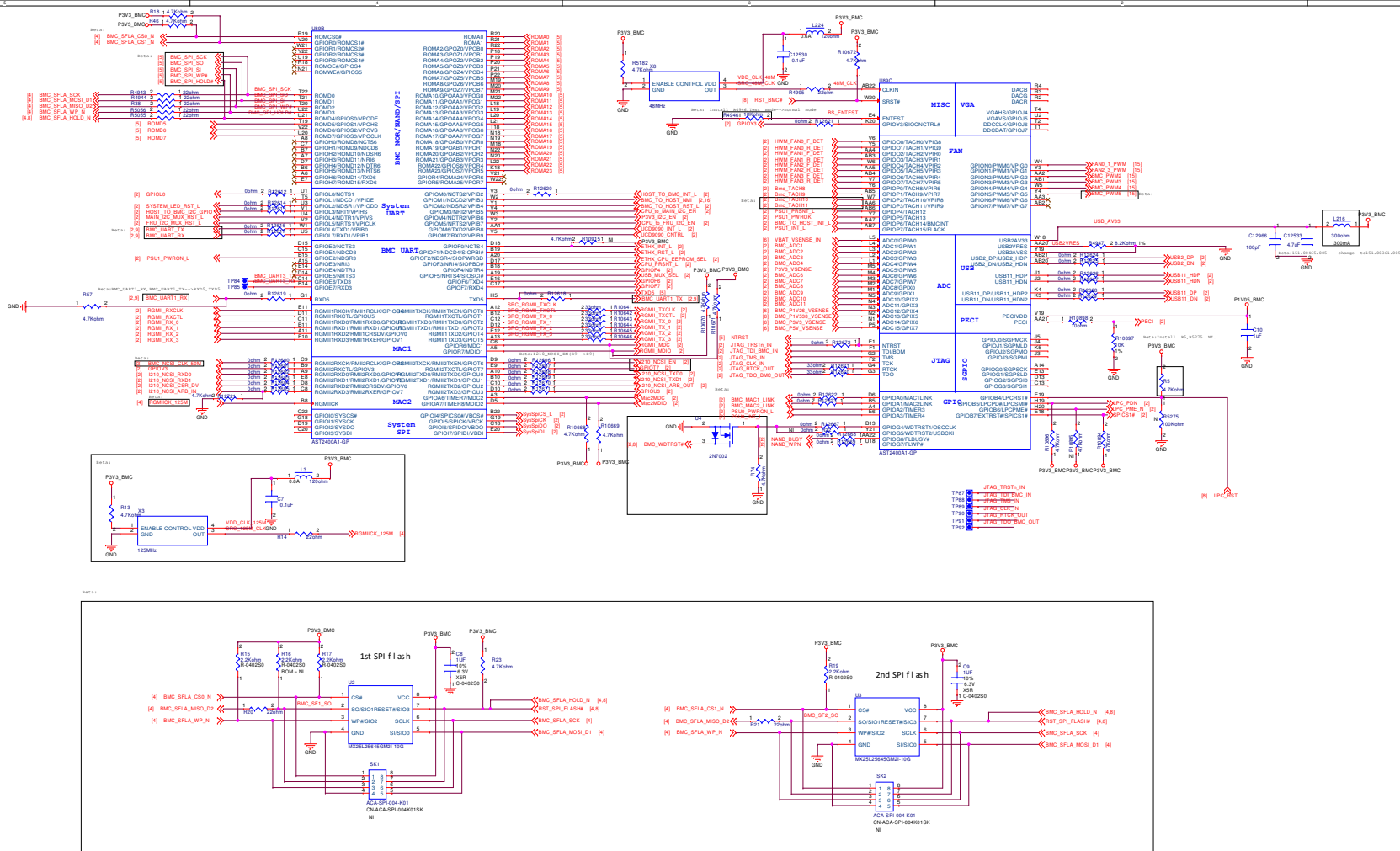
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Core Design

TXD5:Disable ARM ICE reset mode
0 : Enable ICE reset mode
1 : Disable ICE reset mode (default)

NTRST:Reserved

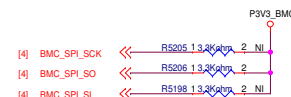


ROMA[1:0] : ARM CPU boot code selection
00 : Boot from NOR flash memory
01 : Boot from NAND flash memory
10 : Boot from SPI flash memory (default)
11 : Disable ARM CPU operation

ROMA[9:8] : H-PLL default clock frequency selection
00: Select 384 MHz (default)
01: Select 360 MHz
10: Select 336 MHz
11: Select 204 MHz

ROMA[17] : Enable BMC 2nd boot watchdog timer
0 : Disable (default)
1 : Enable BMC 2nd boot watchdog timer start counting at power up.
The watchdog timer was located at WDT2.
After watchdog timeout, it will reset BMC and restart booting from the 2nd boot flash at CS1#. CS1# must be the same flash type as CS0# and could be the same firmware as CS0#.

ROMD[2:0]:010:DDR3 SDRAM with CL=6,CWL=5



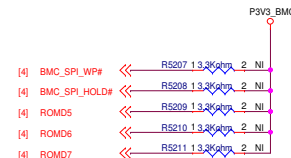
ROMD[7:3] : Reserved for Software DRAM type selection

ROMA[3:2] : VGA memory size selection
00 : Select 8 MB VGA memory
01 : Select 16 MB VGA memory (default)
10 : Select 32 MB VGA memory
11 : Select 64 MB VGA memory

ROMA[11:10] : CPU/AHB clock frequency ratio selection
00 : Select CPU:AHB = 1:1
01 : Select CPU:AHB = 2:1 (default)
10 : Select CPU:AHB = 4:1
11 : Select CPU:AHB = 3:1

Beta:Install R4992
[4] ROMA17 :< R4998 13.2Kohm 2 NI

ROMA[23:18] : Clock source selection
00 : 24 MHz CLKIN
01 : 48 MHz CLKIN (default)
10 : 25MHz CLKIN,24MHz USBCKI
11 : 25MHz CLKIN,48MHz USBCKI



Beta:For A371250 (20180714)



ROMA[4] : Boot flash memory extended option
NOR type flash: data bus width selection
0 : Select 8 bits interface
1 : Select 16 bits interface

SPI type flash: boot address mode selection
0 : Boot with 24 bits address mode (default)
1 : Boot with 32 bits address mode

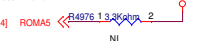
ROMA[13:12] : SPI mode selection
00 : Disable SPI interface (default)
01 : Enable SPI Master
10 : Enable SPI Master and SPI Slave to AHB Bridge
11 : Enable SPI Bypass



ROMA[5] : Enable VGA BIOS ROM
0 : No VGA BIOS ROM (for on-board application) (default)
1 : Enable VGA BIOS ROM (for add-on application)

ROMA[14] : Enable LPC dedicated reset pin function
0 : LPC reset is shared with PCI reset pin(default).
1 : LPC reset is shared with GPIOB4.

Beta:R4976 NI



[4] ROMA14 :< R5046 13.2Kohm 2 NI

Install R5046 for LPC interface.

ROMA[15] : VGA Class Code selection
0 : Select the Class Code for video device
1 : Select the Class Code for VGA device (default)

ROMA[6] : Define MAC\#1 interface
0: RMII/NCSI
1: RGMII (default)



ROMA[16] : SuperIO configuration address selection
0 : Decode 0x2E (default)
1 : Decode 0x4E



ROMA[7] : Define MAC\#2 interface
0: RMII/NCSI (default)
1: RGMII



[4] ROMA18 :< R4990 13.2Kohm 2 NI

[4] ROMA23 :< R4989 13.2Kohm 2 NI

ROMA[19] : Disable ACPI function
0 : Enable ACPI
1 : Disable ACPI (default)

[4] ROMA19 :< R4991 13.2Kohm 2 NI

ROMA[20] : Disable LPC to decode SuperIO 0x2E/0x4E address
0 : Enable address decoding
1 : Disable address decoding (default)

[4] ROMA20 :< R4992 13.2Kohm 2 NI

ROMA[21] : Enable GPIOD pass-through mode
0 : Disable (default)
1 : Enable pass-through at power on

[4] ROMA21 :< R4993 13.2Kohm 2 NI

ROMA[22] : Enable GPIOE pass-through mode
0 : Disable
1 : Enable pass-through at power on (default)

[4] ROMA22 :< R4994 13.2Kohm 2 NI

Beta:R4994 NI

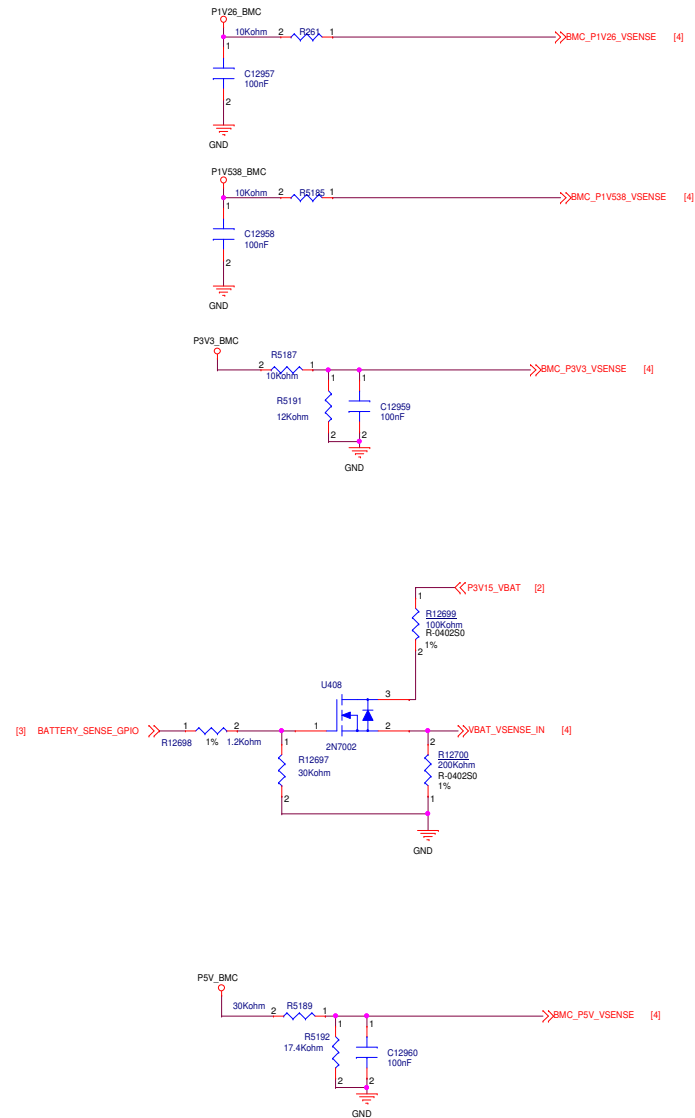
[4] ROMA22 :< R4994 13.2Kohm 2 NI

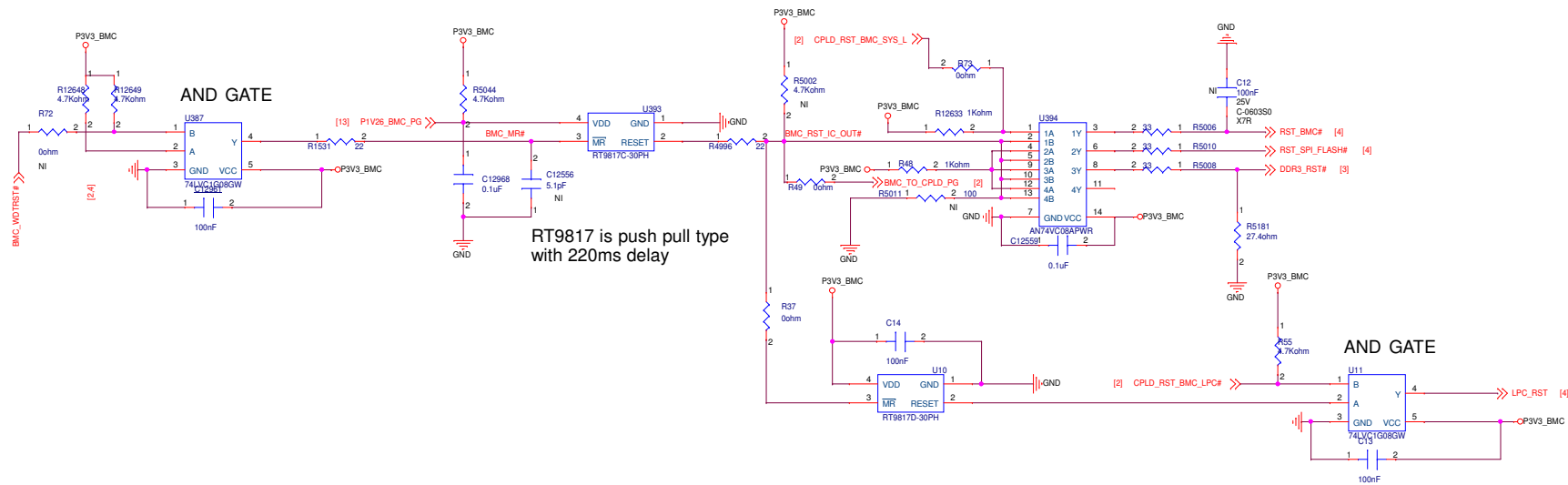
Beta:R4994 NI

<Core Design>

ufiSpace		UfiSpace Co., Ltd.	
Title 5.BMC Strapping			
Document Number: PCB P/N:	1770925T17	Sheet 5 of 17	Rev 025

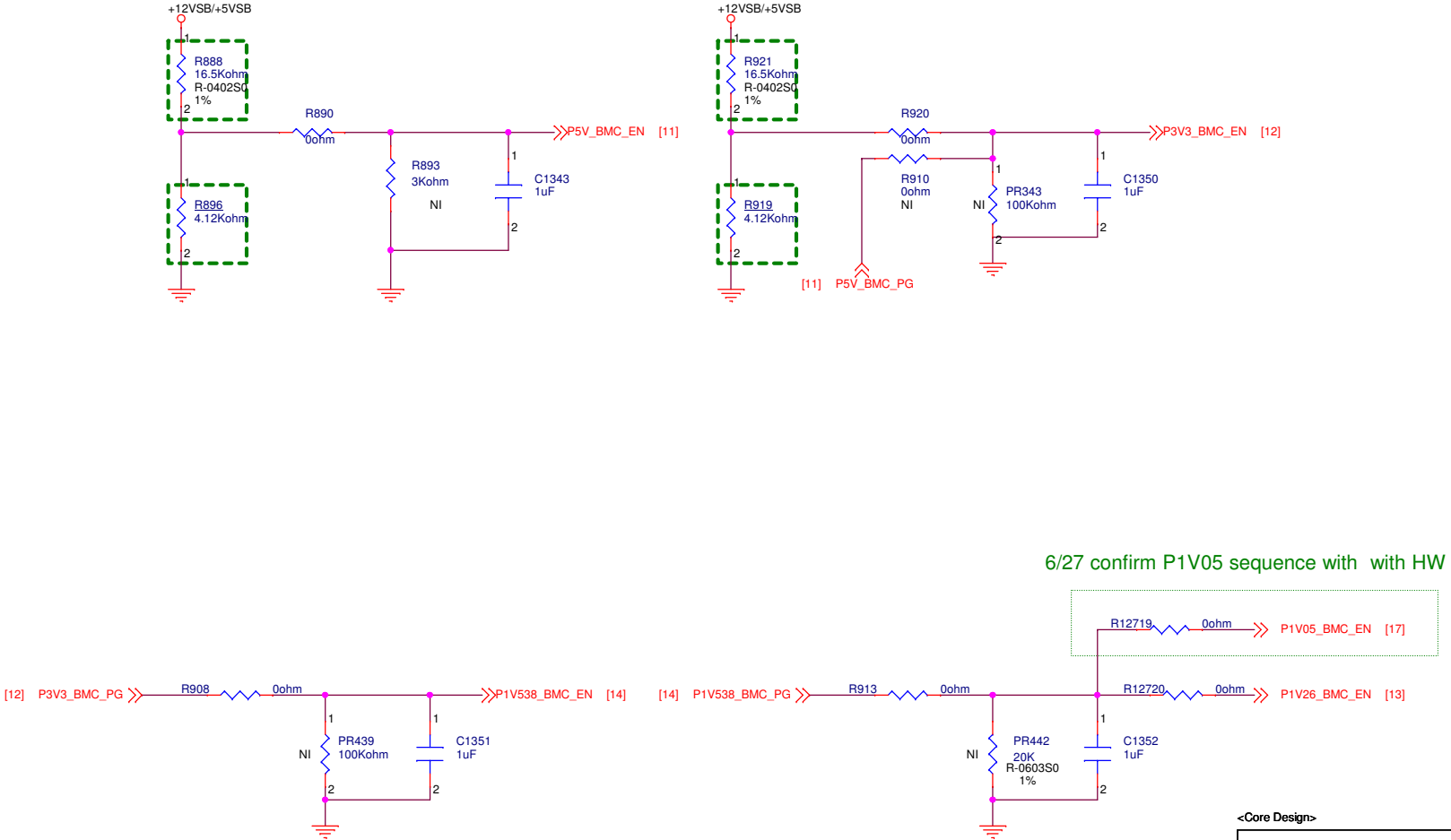
BMC Power Voltage



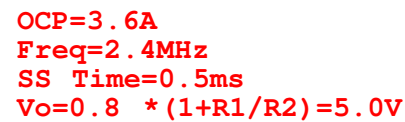


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BMC Power up Sequence



+12VSB/+5VSB



<Core Design>

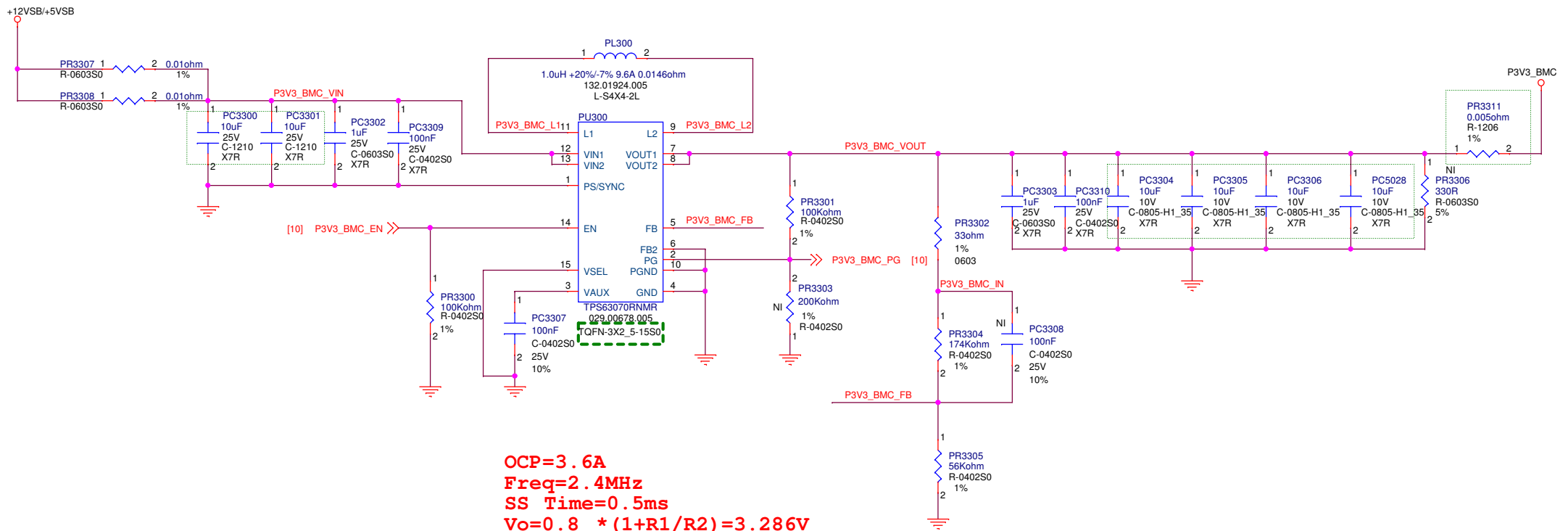
ufiSpace UfiSpace Co., Ltd.

Title **11.12V to 5V_BMC/ 0.5A**

Document Number:
PCB P/N: T770925T17

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P3V3_1.32A



OCP=3.6A
Freq=2.4MHz
SS Time=0.5ms
 $V_o = 0.8 \cdot (1 + R1/R2) = 3.286V$

<Core Design>

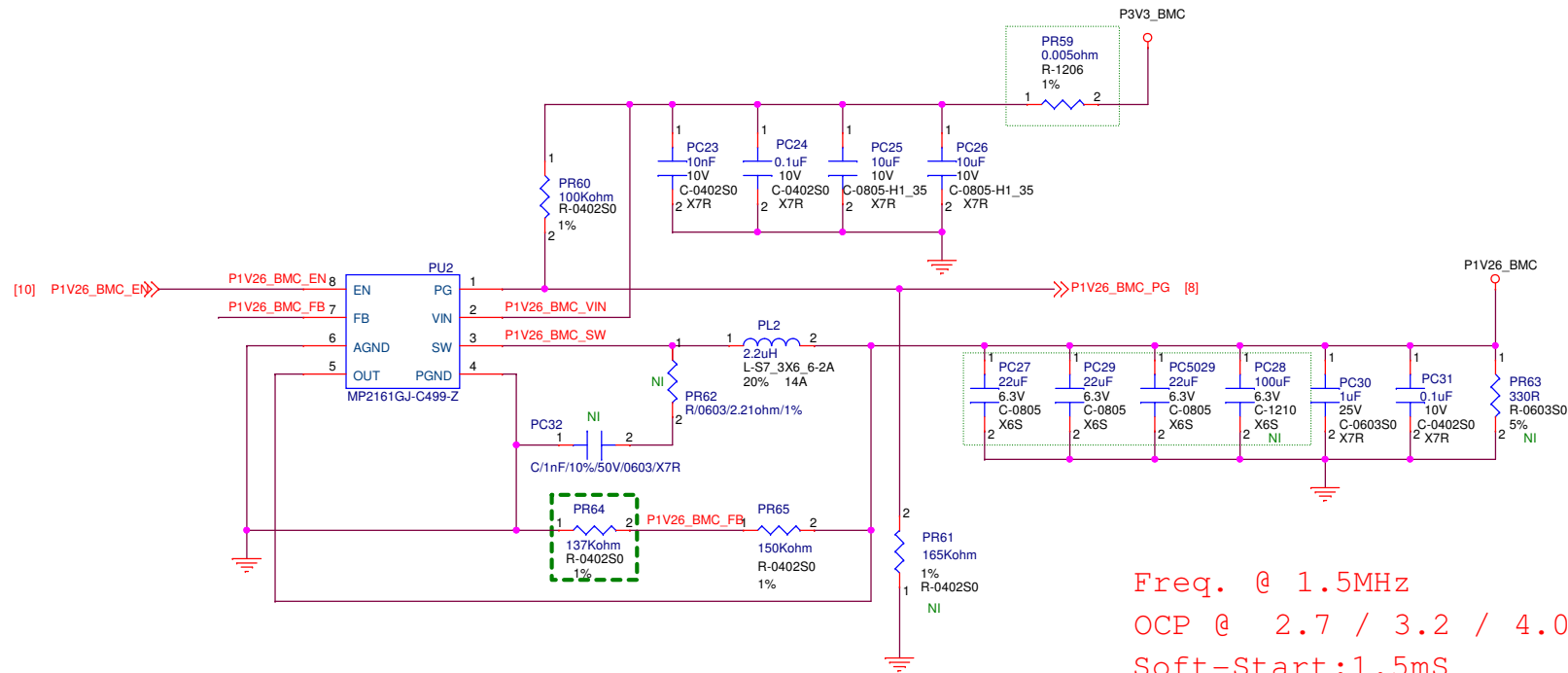
ufiSpace UfiSpace Co., Ltd.

Title	12.12V to 3V3_BMC/1.32A
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Document Number:
PCB P/N: T770925T17

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P1V26_0.766A

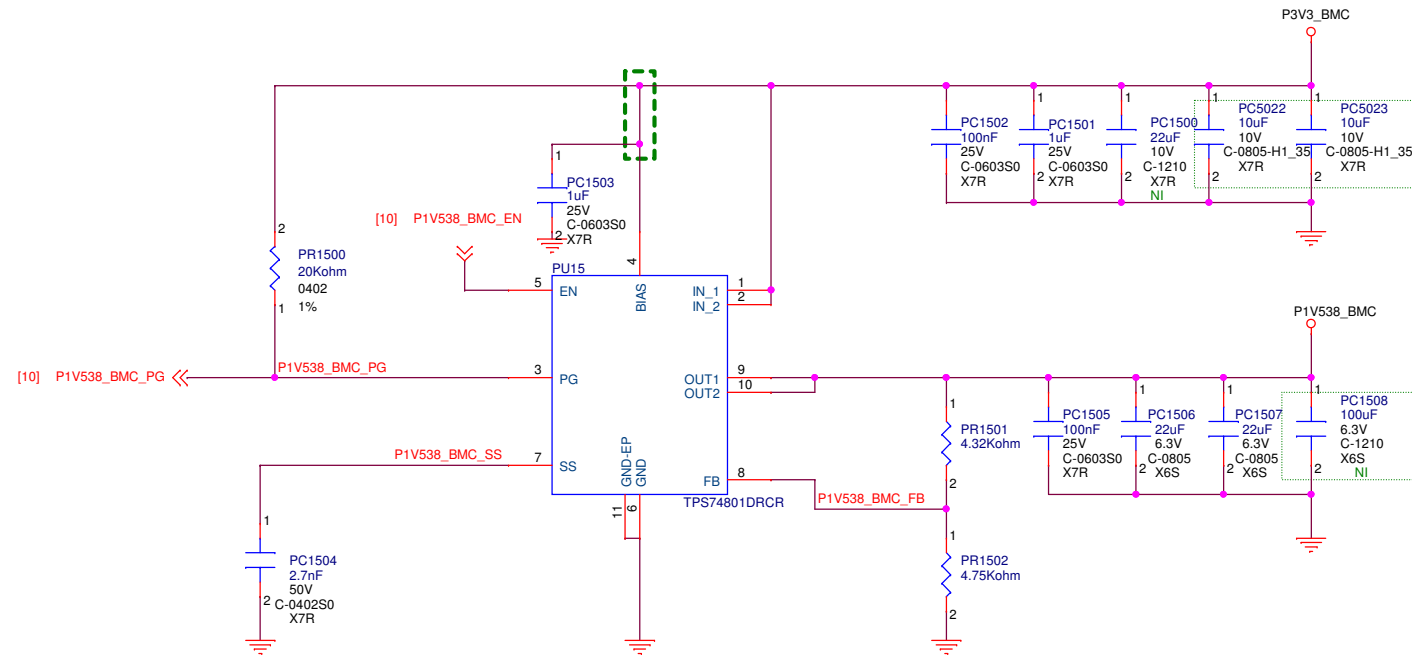


Freq. @ 1.5MHz
 OCP @ 2.7 / 3.2 / 4.0 A
 Soft-Start:1.5mS
 1.26V @0.766A
 $V_o = 0.6 * (1 + PR65/PR64) = 1.257V$

<Core Design>

ufiSpace		UfiSpace Co., Ltd.	
Title			
13.12V to 1V26_BMC/0.766A			
Document Number:		Sheet	Rev
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P1V54_0.36A

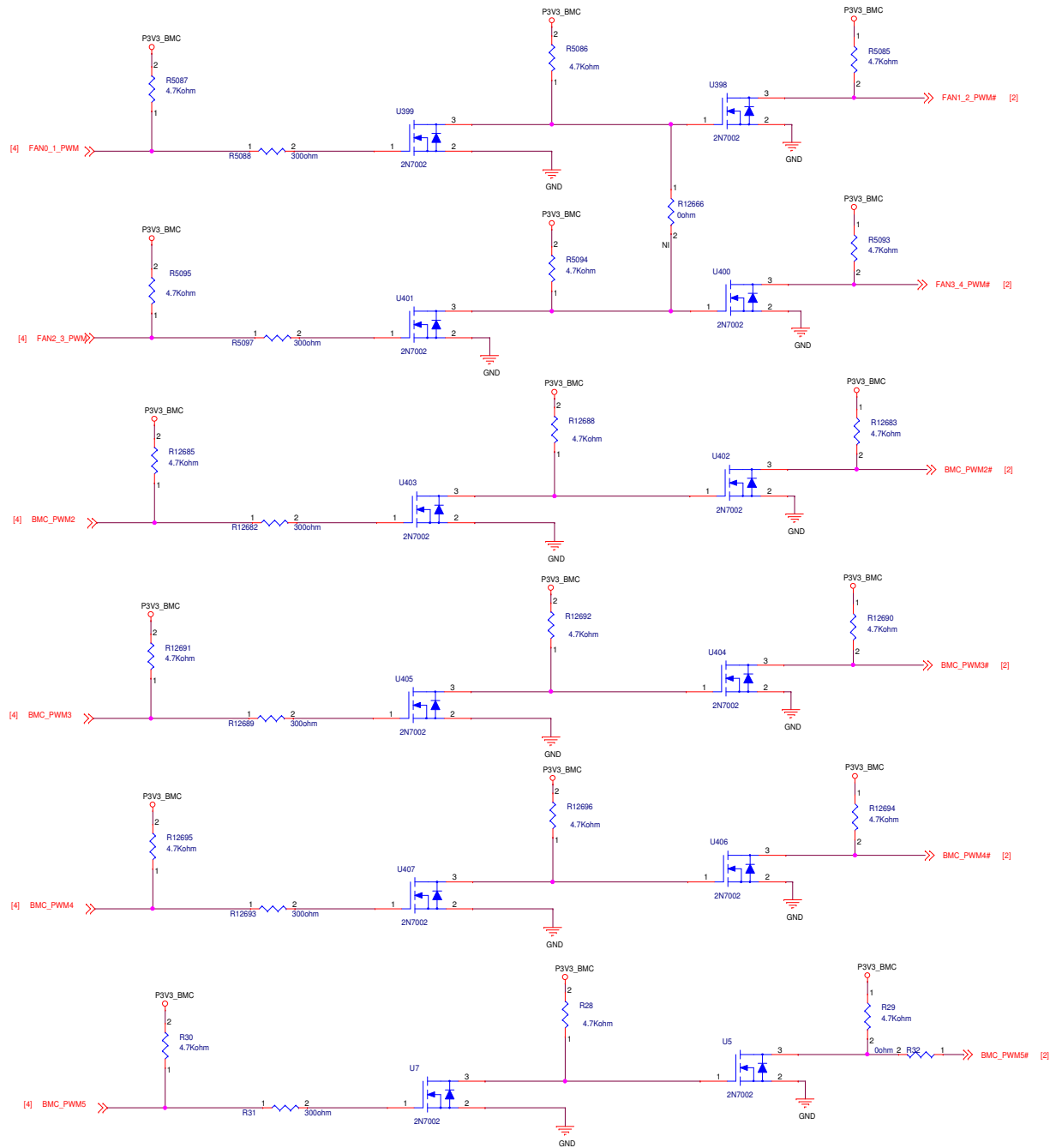


$$V_o = 0.8 * (1 + PR1501 / PR1502) = 1.54V$$

Soft-start Time : 5ms

<Core Design>

		UfiSpace Co., Ltd.	
Title			
14. 3.3V to 1V54_BMC/0.36A			
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<Core Design>

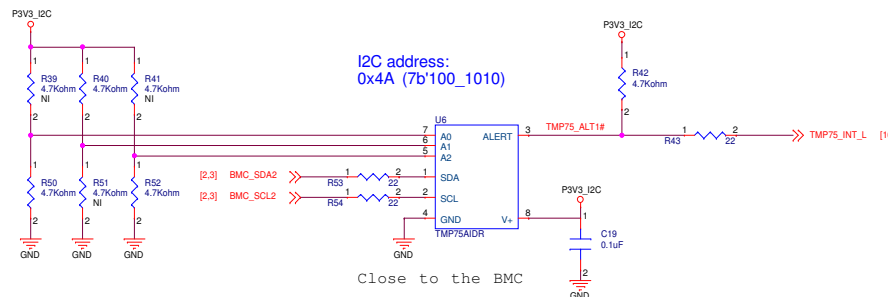
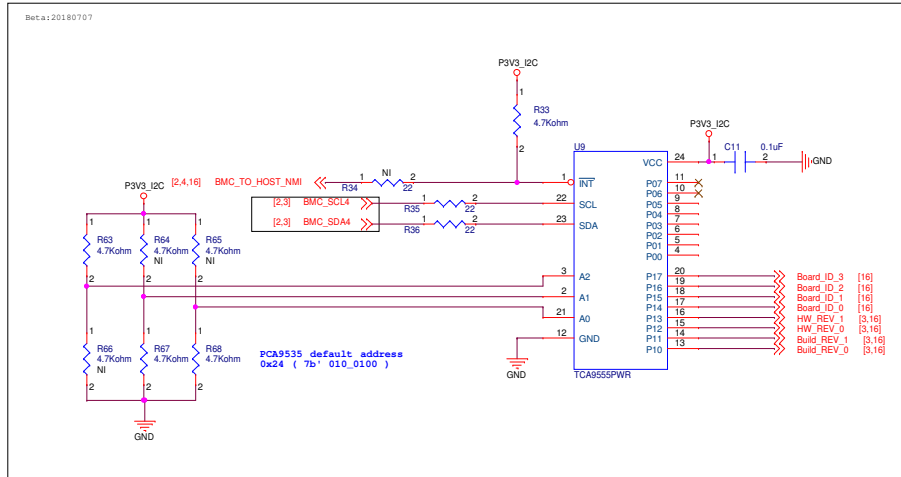
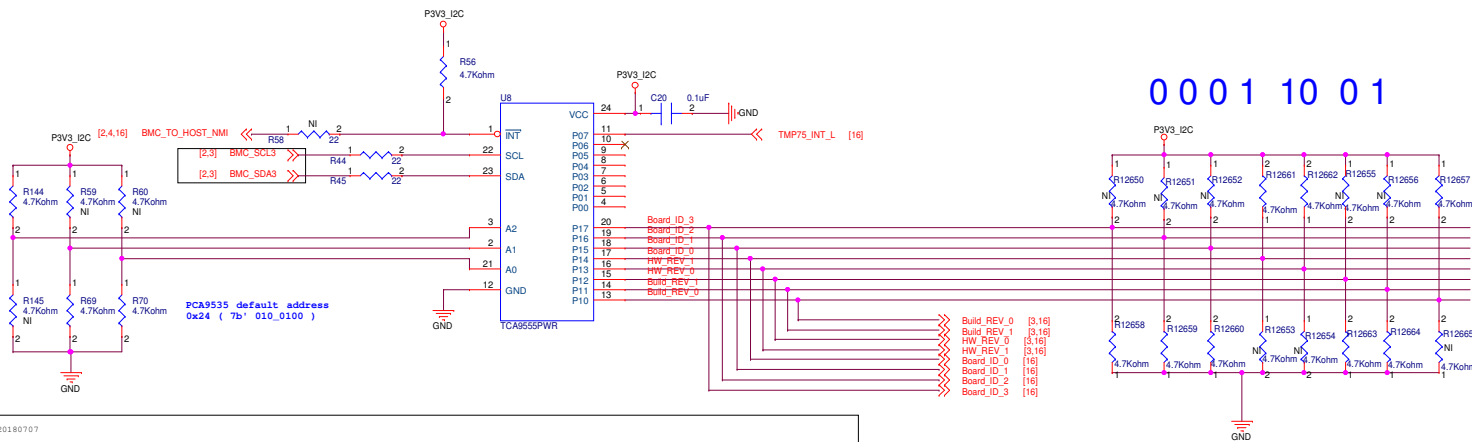
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Title
15.PWM

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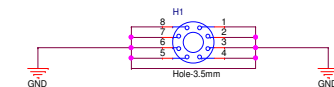


LABEL
 503.00080.005
 LABEL

PCB
 808.03016.025
 PCB

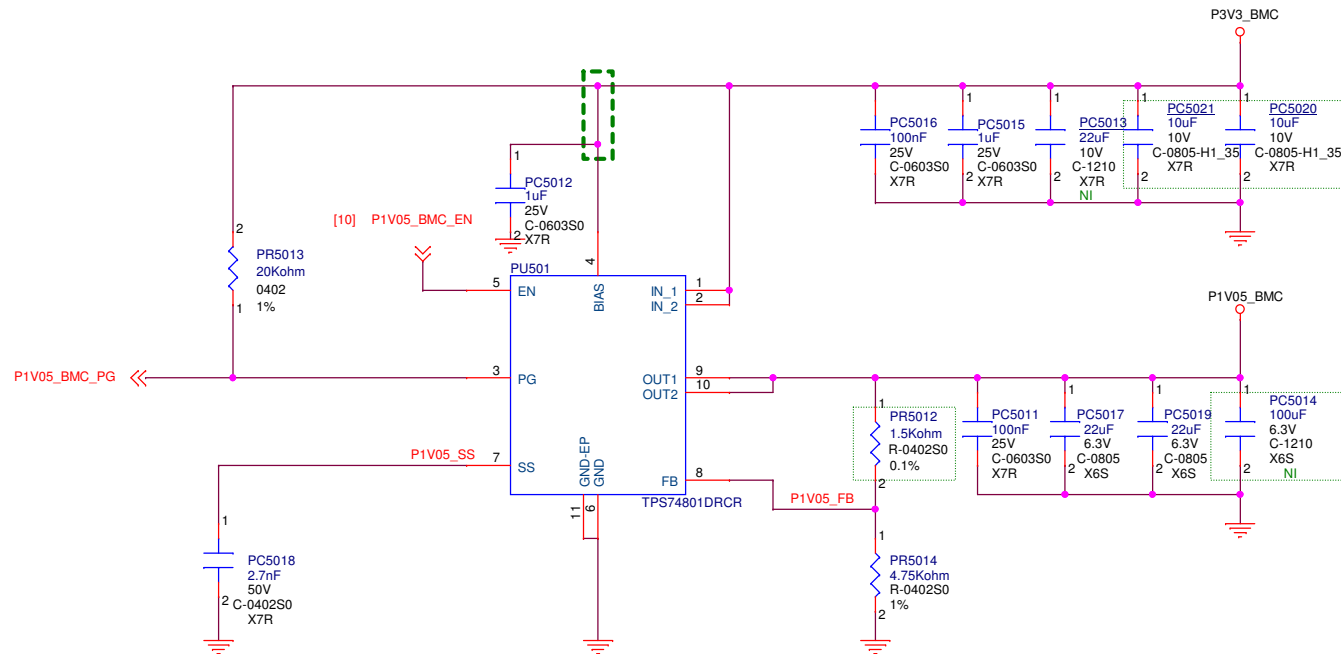
MOUNTING HOLE

Mounting Hole = 3.5mm



<Core Design>

P1V05_0.1A



$$V_o = 0.8 * (1 + PR5012 / PR5014) = 1.05V$$

Soft-start Time : 5ms

<Core Design>

ufiSpace Title 17. 3.3V to 1V05_BMC/0.1A			UfiSpace Co., Ltd.	
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				Rev 025